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1	US 20040103218 A1	20040527	52	Novel massively parallel supercomputer	709/249
2	US 20040012600 A1	20040122	72	Scalable high performance 3d graphics	345/506
3	US 20030221179 A1	20031127	13	System and method for placing clock drivers in a standard cell block	716/18
4	US 20030212975 A1	20031113	14	System and methods for placing clock buffers in a datapath stack	716/10
5	US 20030163750 A1	20030828	17	Clock grid skew reduction technique using biasable delay drivers	713/503
6	US 20030131334 A1	20030710	37	Synthesis strategies based on the appropriate use of inductance effects	716/12
7	US 20030110462 A1	20030612	11	Method for reducing design effect of wearout mechanisms on signal skew in integrated circuit design	716/6
8	US 20030101307 A1	20030529	183	System of distributed microprocessor interfaces toward macro-cell based designs implemented as ASIC or FPGA bread boarding and relative common bus protocol	710/305
9	US 20030074643 A1	20030417	14	Unified database system to store, combine, and manipulate clock related data for grid-based clock distribution design	716/6
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11	US 20030074175 A1	20030417	16	Simulation by parts method for grid-based clock distribution design	703/19
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15	US 6732343 B2	20040504	14	System and methods for placing clock buffers in a datapath stack	716/10
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23	US 6144224 A	20001107	18	Clock distribution network with dual wire routing	326/93
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25	US 5994924 A	19991130	15	Clock distribution network with dual wire routing	326/93

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28	US 5576979 A	19961119	30	Automated development of timing diagrams for electrical circuits	716/6
29	US 5381524 A	19950110	35	Automated development of timing diagrams for electrical circuits	345/804
30	US 5313579 A	19940517	15	B-ISDN sequencer chip device	709/234
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